COOL Chips XII Conference Time Table & Program (Preliminary Ver. Apr. 3)
April 15-17, 2009 @ Yokohama Media & Communication Center, Yokohama, Japan

Wed. 15

Start	End	Duration	Session	Main Hall
13:00	15:30	2:30	Special Invited Lecture 1 	**"Designing Cool Chips Using 3D Stacking Technology"** Yuan Xie Pennsylvania State University, USA Abstract: As technology scales, interconnects have become a major performance bottleneck and a major source of power consumption for nanoscale VLSI chips. One promising option is 3D architectures where a stack of multiple device layers, with Through-Silicon-Vias (TSVs) going through them, are put together on the same chip. As fabrication of 3D integrated circuits has become viable, developing CAD tools and circuit/architectural techniques are imperative to explore the design space for 3D IC design. In this tutorial, a brief introduction on 3D IC integration technology will be given, and the challenges of EDA design tools that can enable the adoption of 3D ICs will be discussed, and the microarchitecture potentials of using 3D technology will be introduced.
15:30	16:00	0:30	Break	
16:00	18:30	2:30	Special Invited Lecture 2 	**"Low power techniques for reconfigurable devices focusing on dynamically reconfigurable processors"** Hideharu Amano Dept. of ICS, Keio University, Japan Abstract: Reconfigurable devices have been widely utilized in embedded systems whose power consumption is essential. Since traditional FPGAs require large power consumption compared with fixed hard-wired logic, it is a main problem for using embedded application. In order to cope with this problem, various types of techniques to reduce the dynamic and leakage power of FPGAs have been proposed. On the contrary, the dynamically reconfigurable processors achieve 8-10 times lower energy computation compared with DSPs with corresponding technologies, and it is the main motivation to be used in consumer products. In this session, first, the power of both FPGAs and dynamically reconfigurable processors are analyzed, and the difference caused by their architectures is discussed. Then, various power reduction methods including operand isolation, reducing dynamic reconfiguration, controlling Vdd, dual Vdd, dual Vth and power gating are reviewed, and application to reconfigurable devices is discussed.

Thu. 16

Start	End	Duration	Session	Main Hall
9:30	9:50	0:20	Session I	Welcome & Opening Remarks
9:50	10:40	0:50	(continuation) 	**Keynote Presentation 1** **"Cisco QFP - Quantum Flow Processor -"** Will Eartherton Cisco Systems inc, ERBU Director Engineering, USA Abstract: Cisco has seen a growing need for Service Providers to handle the growing amount of traffic and complexity of network traffic then decided to create its own networking chipset called "Cisco QFP - Quantum Flow Processor". Cisco QFP is the most advanced networking silicon and the first fully integrated programmable networking chipset which consists of 40 cores, has 800 million transistor density and can perform up to 160 simultaneous processes. Cisco QFP is powering the date plane engine of Cisco ASR1000 Series Aggregation Service Router which is suitable at network edge for IP NGN and Enterprise Network with its high performance, versatile functionality, high availability, less space and power efficiency. In this keynote, Cisco QFP architecture and its applications are introduced.

10:40	11:30	0:50	(continuation) 	**Keynote Presentation 2** **"New 3-D Integration Technology and 3-D Systems"** Mitsumasa Koyanagi Department of Bioengineering and Robotics, Tohoku University, Japan Abstract: A three-dimensional (3-D) integration technology based on the wafer-to-wafer bonding using Through-Silicon Vias (TSV's) has been developed. A 3-D image sensor chip, 3-D shared memory chip, 3-D artificial retina chip and 3-D microprocessor test chip have been fabricated by using this technology. In the wafer-to-wafer 3-D integration technology, however, the overall chip yield exponentially decreases with an increase in the number of stacked layers. To solve these problems, we have proposed a new 3-D integration technology called super-chip integration in which more than one thousand of known good dies (KGD's) are simultaneously aligned and bonded onto chips on a wafer using a self-assembly technique.
11:30	11:50	0:20	Break	
11:50	12:20	0:30	Session II	Poster Short Speech Session Chair: Masanori Muroyama (Tohoku Univ., Japan)
12:20	13:40	1:20	Lunch	
13:40	14:30	0:50	Session III Session III-1(R) Session III-2(R)	**Video Codec** Session Co-Chairs: Hideki Ymauchi (SAMSUNG, Korea) and Hiroaki Nakata (Hitachi, Japan) **"A Low-Power H.264/AVC Codec with 1080p/60 Processing Capabilities"** Hidetoshi Matsumura, Tatsushi Ootsuka, Yasuhiro Watanabe, Ryuji Fujita, Akira Nakagawa, and Hiroshi Nakayama Fujitsu Laboratories Ltd., Japan **"An 176mW Full-HD Multi-Standard Video Codec for Mobile Application Processors"** Motoki Kimura, Kenichi Iwata, Seiji Mochizuki, Hiroshi Ueda, Masakazu Ehama, and Hiromi Watanabe, Renesas Technology Corp., Japan
14:30	15:10	0:40	Session IV Session IV-1(R) Session IV-2(S)	**Software Defined Radio Processors** Session Co-Chairs: Masaaki Kondo (UEC, Japan) and Yuichiro Shibata (Nagasaki Univ., Japan) **"Flexible Correlation Accelerator for a Multiple-mode Baseband Processor"** Toshiki Takeuchi and Hiroyuki Igura NEC Corporation, Japan **"Multi-Processor SDR Platform with HW Supported Dynamic Scheduling"** Emil Matúš, Torsten Limberg, Markus Winter, Marcel Bimberg, Reimund Klemm, Marcos B.S. Tavares, Hendrik Ahlendorf, and Gerhard Fettweis Technische Universität Dresden, Germany
15:10	16:10	1:00	Break (Poster)	

16:10	17:30	1:20	Session V Session V-1(R) Session V-2(S) Session V-3(S) Session V-4(R)	**Multi Core** Session Co-Chiars: Gyungho Lee (Korea Univ., Korea) and Keiji Kimura (Waseda Univ., Japan) **"Low Power Design of a High Performance Quad-core Microprocessor for Mission Critical Servers"** Ryuji Kan, Tatsumi Nakada, Yoshihiko Satsukawa, and Gaku Ito Fujitsu Ltd., Japan **"Hybrid Communication-Aware Task Scheduling for Energy Minimization in On-Chip Multiprocessor"** HyunJin Kim, Seongyong Ahn, Hyejeong Hong, Hong-Sik Kim, and Sungho Kang Yonsei University, Korea **"Ultra Android: High Energy Efficiency Parallel Java Objects Processing via Object Request Broker on Heterogeneous Multi-core Processor"** Takeshi Ohkawa, Yukoh Matsumoto, and Kenji Toda National Institute of Advanced Industrial Science and Technology (AIST), Japan **"Domain Partitioning Technology for Embedded Multi Core Processors"** Tohru Nojiri, Yuki Kondo, Naohiko Irie, and Hideo Maejima Hitachi Ltd., Japan
17:30	18:30	1:00	Poster discussion	

Fri. 17

Start	End	Duration	Session	Main Hall
9:30	10:20	0:50	Session VI 	**Keynote Presentation 3** **"Future Robotics and the Key Components"** Hiroshi Ishiguro Department of Adaptive Machine Systems, Osaka University ATR Intelligent Robots and Communication Laboratories Abstract: Many robotics researchers are exploring new possibilities of intelligent robots in our everyday life. Humanoid and androids, which have various modalities, interact and communicate with humans as new information media for providing various daily services. This talk introduces a series of robots developed in ATR Intelligent Robotics and Communications Laboratories and Department of Adaptive Machine Systems, Osaka University and discusses the fundamental issues. One of the fundamental issues is the hardware development. The reliable and low cost robots expected to work in our future society requires various computer chips for handling sensory information and controls the behaviors. This talk also discusses what kinds of chips are expected for developing the future robots that works in our town and home.
10:20	10:40	0:20	Break (Poster)	

10:40	12:20	1:40	Session VII	**Recognition Processors** Session Co-Chairs: Yuetsu Kodama (AIST, Japan) and Fumio Arakawa (Renesas Technology)
			Session VII-1(R)	**"A 320 x 240 Pixel Smart Image Sensor for Object Identification and Pose Estimation"** Atsushi Iwashita, Takashi Komuro, and Masatoshi Ishikawa University of Tokyo, Japan
			Session VII-2(R)	**"Architecture Design of Versatile Recognition Processor for Sensornet Applications"** Yuya Hanai, Yuichi Hori, Jun Nishimura, and Tadahiro Kuroda Keio University, Japan
			Session VII-3(R)	**"An Energy Efficient Real-Time Object Recognition Processor with Neuro-Fuzzy Controlled Workload-aware Task Pipelining"** Joo-Young Kim, Minsu Kim, Seungjin Lee, Jinwook Oh, Kwanho Kim, Jeong-Ho Woo, and Hoi-Jun Yoo Korea Advanced Institute of Science and Technology (KAIST), Korea
			Session VII-4(R)	**"A 128-Parallel SIMD Image Signal Coprocessor with High Area Efficiency"** Keiri Nakanishi, Shunichi Ishiwata, Katsuyuki Kimura, Takahisa Wada, Masato Sumiyoshi, Yasuki Tanabe, Takashi Miyamori, and Yoshiro Tsuboi Toshiba Corporation, Japan
12:20	13:40	1:20	Lunch	
13:40	14:20	0:40	Session VIII 	**Invited Presentation** **"STP Engine, a C-based Programmable HW Core featuring Massively Parallel and Reconfigurable PE Array: its Architecture, Tool, and System Implications"** Masato Motomura 1st SOC Operations Unit, NEC Electronics Abstract: Stream Transpose (STP) Engine is a programmable HW core to accelerate stream processing in modern system LSIs. It is composed of an array of numerous numbers of processing and memory elements as well as an intelligent data streaming HW mechanism. Key differentiation from other many-core type parallel architectures lies in its programming model: i.e., a design tool based on high-level HW synthesis technology compiles a C source code into a set of pseudo HW configurations which are spatially mapped onto the array. The STP engine is productized in 90nm-generation system LSIs, and is targeted for wider-range use in forthcoming generations beyond 40nm. This talk covers the core's architecture and tool issues, as well as its real world system applications.
14:20	14:40	0:20	Break (Poster)	
14:40	15:50	1:10	Session IX	**Processing Elements** Session Co-Chairs: Kyoung-Rok Cho (Chungbuk National Univ. Korea) and Koji Hirairi (Sony, Japan)
			Session IX-1(R)	**"Optical Multi-Drop Memory Architecture for Multi-Core Processors"** A. Okazaki and Y. Katayama IBM Tokyo Research Laboratory, Japan
			Session IX-2(S)	**"Improving Effectiveness of Pipeline Stage Unification via ALU Cascading"** Jun Yao, Hajime Shimada, Kosuke Ogata, Shinobu Miwa, and Shinji Tomita Kyoto Univ., Japan
			Session IX-3(S)	**"A Leakage-Aware L2 Cache Management Technique for Producer-Consumer Sharing in Low-Power Chip Multiprocessors"** Hyunhee Kim and Jihong Kim Seoul National University, Korea
			Session IX-4(S)	**"L2 cache way prediction techniques for low-power MPSoC design"** Chun-Mok Chung and Jihong Kim Seoul National University, Korea
15:50	16:00	0:10	Break	

16:00	18:00	2:00	Session X	**Panel Discussion** **Title: "How can Cool Chips contribute ROBOTICS that support our future electronics industry?"** Organizer/Moderator: Yoshiaki Hagihara (AIPS, Japan) Panelists: Nobuyuki Yamazaki (Keio Univ., Japan) Takashi Komuro (Univ. of Tokyo, Japan) Yoshiaki Hagihara (AIPS, Japan) Fumio Arakawa (Renesas Technology, Japan) Abstract: Voice Recognition, Image Recognition, and Embedded Robotics System Developments are essentials of the Artificial Intelligent Partner System (AIPS) Solutions. This panel will be focused on the life style that we will see 5 to 10 years from now. Each experts will be asked to present his personal view of how the Cool Chips and Cool Software Community will have important roles to contribute AIPS ROBOTICS that will change our future life style completely, and in return will support our future electronics industry.
18:00	18:10	0:10		Closing Remarks

Poster Program

Poster 1	**Performance Impact of On-Chip SRAMs in an OpenVG Accelerator** Yong-Luo Shen and Hyeong-Cheol Oh (Korea University, Korea)
Poster 2	**Efficiency of DVFS Techniques for Memory-Bound Real-Time Applications** Hyung Beom Jang and Sung Woo Chung (Korea University, Korea)
Poster 3	**Asynchronous Control of Multi-Core Systems** Slawomir Mikula and Andrzej Kos (AGH University of Science and Technology, Poland)
Poster 4	**CG Application Domain Specific Heterogeneous Multi-Core Architecture and Software corresponds to 800TFLOPS of processing** Yukoh Matsumoto, Yoshinori Ogata, and Motohisa Tominaga (TOPS Systems, TOYOTA, and Nihon Unisys)
Poster 5	**A Self-Timed Delay Cell Structure for Prototyping Asynchronous Circuits** Young Woo Kim and Seongwoon Kim (Electronics and Telecommunications Research Institute, Korea)
Poster 6	**A Tagless and Efficient Cache Design in Embedded Systems** Ching-Wen Chen, Chang-Jung Ku, and Chun-Hung Lin (Feng Chia University, Taiwan)
Poster 7	**A Linear Array VLIW Processor for Image Processing** Munehisa Agari, Takashi Nakada, and Yasuhiko Nakashima (Nara Institute of Science and Technology)
Poster 8	**A Preliminary Study on Dynamic Core Resource Allocation Mechanism for Flexible Multicore Architecture** Yusuke Yamada, Ryotaro Kobayashi, Yuhta Wakasugi, and Kenji Kise (Toyohashi University of Technology and Tokyo Institute of Technology)
Poster 9	**Low-Power Variable-Pipeline Router using Pipeline-Stage Integration** Yuto Hirata, Hiroki Matsutani, Michihiro Koibuchi, and Hideharu Amano (Keio University and National Institute of Informatics)
Poster 10	**A Proposal of Low Power and Less costly Soft Error Correction Mechanism for Microprocessors** Tomonari Muneoka and Ryotaro Kobayashi (Toyohashi University of Technology)
Poster 11	**A Preliminary Study on Adaptable Data Access Support for Manycore** Tomohide Takahashi, Ryotaro Kobayashi, Akira Moriya, and Kenji Kise (Toyohashi University of Technology and Tokyo Institute of Technology)
Poster 12	**Design of Asynchronous Instruction Cache for an Embedded Microcontroller** Kwang -Bae Jeon, Seok-Man Kim, Je-Hoon Lee Myeong-Hoon Oh, and Kyoung-Rok Cho (Chungbuk National University and ETRI, Korea)
Poster 13	**Design and Evaluations of Prototype SMA: A Massive Array of Low-Energy Reconfigurable Processor** Yoshihiro Yasuda, Yoshiki Saito, Kyundong Kim, Tunbunheng Vasutan, and Hideharu Amano (Keio University and University of Tokyo)
Poster 14	**An FPGA Implementation of Vector Graphics Core** Jinhong Park, Jinwoo Kim, Yong-jin Park, Cheolho Jeong, Youngsik Kim, Woo-Chan Park, and Tack-Don Han (Yonsei University, Sejong University, Korea Polytechnic University, and mGine)
Poster 15	**ScalableCore : High-Speed Prototyping System for Many-Core Processors** Shinya Takamaeda, Shimpei Watanabe, Shimpei Sato, Koh Uehara, Yuhta Wakasugi, Naoki Fujieda, Yosuke Mori, and Kenji Kise (Tokyo Institute of Technology)
Poster 16	**An Efficient Register Remapping Technique for Stack-based Hardware Virtual Mach** Jong-Sung Lee, Kwang-Ho Lee, and Hyun-Gyu Kim (Advanced Digital Chips, Korea)

Poster 17	**Can Conventional Hardware Prefetchers Work Well for Multicores?** Naoto Fukumoto, Koji Inoue, and Kazuaki Murakami (Kyushu University)
Poster 18	**Low Energy Hashing Hardware for String Pattern Matching** E.-K. Hong, S.-T. Paek, I.-H. Choi, and H.-C. Oh (Korea University and Somansa, Korea)
Poster 19	**Early Evaluation of a Memory-Stacked Vector Processor** Yusuke Funaya, Ryusuke Egawa, Hiroyuki Takizawa, and Hiroaki Kobayashi (Tohoku University)
Poster 20	**Geyser-1: A CPU with Fine-grain Power Gating** Daisuke Ikebuchi, Naomi Seki, Yu Kojima, Masahiro Kamata, Lei Zhao, Hideharu Amano, Toshiaki Shirai, Satoshi Koyama, Tatsunori Hashida, Yusuke Umahashi, Hiroki Masuda, Kimiyoshi Usami, Seidai Takeda, Hiroshi Nakamura, Mitaro Namiki, and Masaaki Kondo (Keio University, Shibaura Institute of Technology, University of Tokyo, Tokyo University of Agriculture and Technology and University of Electro-Communications)
Poster 21	**A Low-Leakage Routing Table Design** Yen-Jen Chang (National Chung Hsing University, Taiwan)
Poster 22	**An Implementation of Ray Tracer on V5 FPGA** Woochan Park, Jinseok Hur, Dongseok Kim, Jaeho Nah, Jeongsu Park, Jinhong Park, and Tackdon Han (Sejong University and Yonsei University, Korea)
Poster 23	**Evaluation of arithmetic precision for an FPGA-based reconfigurable DC-DC converter** Masato Soejima, Syohei Sukita, Yuichiro Shibata, Fujio Kurokawa, Tsuyoshi Hamada, Tomonari Masada, and Kiyoshi Oguri (Nagasaki University)
Poster 24	**FPGA implementation of packet header lookup** Young Choi, E.-K. Hong, S.-T. Paek, and Hyeong-Cheol Oh (Korea University and Somansa, Korea)
Poster 25	**Dynamic optically reconfigurable gate array with high defect tolerance** Daisaku Seto and Minoru Watanabe (Shizuoka University)
Poster 26	**Power reduction effect of an inversion/non-inversion dynamic optically reconfigurable gate array** Shinichi Kato and Minoru Watanabe (Shizuoka University)